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EXAMINER	
ROLAND, CHRISTOPHER M	
ART UNIT	PAPER NUMBER
2893	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/573,458	OTSUKA ET AL.	
	Examiner	Art Unit	
	Christopher M. Roland	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6 and 8-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6 and 8-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 August 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 26 February 2009 has been entered.

Status of the Claims

2. Amendment filed 26 February 2009 is acknowledged. **Claims 1-4, 6, 8, 9, 11** have been amended. **Claim 12** has been added. **Claims 1-4, 6, and 8-12** are pending.

Claim Objections

3. **Claims 2 and 3** are objected to because of the following informalities:

Claim 2 recites the limitation, “and a distance that allows a quantum mechanical tunnel effect with the two dimensional carrier to be obtained.” This is believed to be merely a typographical error and that Applicant intends, “and is formed to a distance that allows a quantum mechanical tunnel effect with the two dimensional carrier to be obtained.”

Claim 3 recites the limitation, "a first interface between the third semiconductor layer and the second semiconductor layer." Claim 3 further recites, "the first interface between the first semiconductor layer and the second semiconductor layer." The claim renders indefinite between which two semiconductor layers the interface is formed. As best understood by Examiner, the third semiconductor layer is sandwiched between the first semiconductor layer and the second semiconductor layer such that an interface between the first semiconductor layer and the second semiconductor layer does not exist.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claims 1-4, 6, and 8-12** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-4, 6, and 8-10 recite the limitation, "a primary surface of the second semiconductor layer." It is unclear as to which surface: top, bottom, or side, is the primary surface.

Comment [D1]: Is this really a 112? Isn't this similar to him saying "first surface?

Claims 11 and 12 are rejected for merely containing the flaw(s) of the parent claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1, 3, and 11** are rejected under 35 U.S.C. 102(b) as being anticipated by Peatman et al. ("A Novel Schottky/2-DEG Diode for Millimeter- and Submillimeter-Wave Multiplier Applications," hereinafter Peatman) of record.

With respect to claim 1, as best understood by Examiner, Peatman teaches (FIG. 1) a semiconductor device as claimed, comprising:

a first semiconductor layer (InGaAs layer) that is formed from a first semiconductor material (p. 12, col. 1, ln. 32-48);

a second semiconductor layer (AlGaAs layer) that is formed from a second semiconductor material on the first semiconductor layer (p. 12, col. 1, ln. 32-48);

a two-dimensional carrier (2-DEG) that is formed within the first semiconductor layer and in the vicinity of an interface between the first semiconductor layer and the second semiconductor layer (p. 12, col. 1, ln. 32-48);

a first concave portion (trench) that is formed penetrating at least the second semiconductor layer from a primary surface of the second semiconductor layer, and is formed from the interface to a predetermined depth in the first semiconductor layer (p. 12, col. 1, ln. 32-48);

a first electrode (Schottky contact) that is formed on a bottom surface and side surface of the first concave portion and that forms a Schottky junction to the semiconductor layers which contact the bottom surface and the side surface of the first concave portion (p. 12, col. 1, ln. 32-48); and

a second electrode (ohmic contact) that is formed in an area of the second semiconductor layer that is located away from the first electrode and that forms a low resistance contact with the second semiconductor layer (p. 12, col. 1, ln. 32-48),

wherein:

the primary surface of the second semiconductor layer faces the interface between the first semiconductor layer and the second semiconductor layer (p. 12, col. 1, ln. 32-48); and

the side surface of the first concave portion is inclined against the interface (p. 12, col. 1, ln. 32-48).

With respect to claim 3, as best understood by Examiner, Peatman teaches (FIG. 1) a semiconductor device as claimed, comprising:

a first semiconductor layer (InGaAs layer) that is formed from a first semiconductor material (p. 12, col. 1, ln. 32-48);

a second semiconductor layer (GaAs layer) that is formed from a second semiconductor material above the first semiconductor layer (p. 12, col. 1, ln. 32-48);

a third semiconductor layer (AlGaAs layer) that is sandwiched between the first semiconductor layer and the second semiconductor layer and that is formed having a

thickness that allows a quantum mechanical tunnel effect to be obtained (p. 12, col. 1, ln. 32-48);

a two-dimensional carrier (2-DEG) that is formed within the first semiconductor layer and on the third semiconductor layer side of the first semiconductor layer (p. 12, col. 1, ln. 32-48);

a first concave portion (trench) that is formed penetrating at least the second semiconductor layer from a primary surface of the second semiconductor layer, and is formed from a first interface between the third semiconductor layer and the second semiconductor layer to a predetermined depth in the first semiconductor layer (p. 12, col. 1, ln. 32-48);

a first electrode (Schottky contact) that is formed on a bottom surface and side surface of the first concave portion and that forms a Schottky junction with the semiconductor layers which contact the bottom surface and the side surface of the first concave portion (p. 12, col. 1, ln. 32-48); and

a second electrode (ohmic contact) that is formed in an area of the second semiconductor layer that is located away from the first electrode and that forms a low resistance contact with the second semiconductor layer (p. 12, col. 1, ln. 32-48),

wherein:

the primary surface of the second semiconductor layer faces the first interface between the first semiconductor laver and the second semiconductor layer (p. 12, col. 1, ln. 32-48); and

the side surface of the first concave portion is inclined against a second interface between the first semiconductor layer and the third semiconductor layer (p. 12, col. 1, ln. 32-48).

With respect to claim 11, as best understood by Examiner, Peatman teaches wherein a forward current passes from the first electrode to the second electrode when a voltage is applied from the first electrode to the second electrode, and a reverse current passing from the second electrode to the first electrode is restricted when the voltage is applied from the first electrode to the second electrode (p. 12, col. 1, ln. 32-48).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 2 and 8-11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Peatman in view of Kanazawa (Japanese Patent Application Publication 03-016179, hereinafter Kanazawa ‘179) of record.

With respect to claim 2, as best understood by Examiner, Peatman teaches a semiconductor device substantially as claimed, comprising:

a first semiconductor layer (InGaAs layer) that is formed from a first semiconductor material (p. 12, col. 1, ln. 32-48);

a second semiconductor layer (AlGaAs layer) that is formed from a second semiconductor material on the first semiconductor layer (p. 12, col. 1, ln. 32-48);

a two-dimensional carrier (2-DEG) that is formed within the first semiconductor layer and in the vicinity of an interface between the first semiconductor layer and the second semiconductor layer (p. 12, col. 1, ln. 32-48);

a first concave portion (trench) that is formed from a primary surface of the second semiconductor layer reaching at least the interface, and a distance that allows a quantum mechanical tunnel effect with the two dimensional carrier to be obtained (p. 12, col. 1, ln. 32-48);

a first electrode (Schottky contact) that is formed on a bottom surface and a side surface of the first concave portion and that forms a Schottky junction to the semiconductor layers which contact therewith (p. 12, col. 1, ln. 32-48); and

a second electrode (ohmic contact) that is formed in an area of the second semiconductor layer that is located away from the first electrode and that forms a low resistance contact with the second semiconductor layer (p. 12, col. 1, ln. 32-48),

wherein:

the primary surface of the second semiconductor layer faces the interface between the first semiconductor layer and the second semiconductor layer (p. 12, col. 1, ln. 32-48); and

the side surface of the first concave portion is inclined against the interface (p. 12, col. 1, ln. 32-48).

Thus, Peatman is shown to teach all the features of the claim with the exception of wherein the first electrode is also formed on the primary surface of the second semiconductor layer surrounding the first concave portion.

However, Kanazawa '179 teaches (FIG. 1) a first electrode formed on the primary surface of an second semiconductor layer (11) directly above a first semiconductor layer (10) to generate a two-dimensional electron gas in said first semiconductor layer in a device whose conversion loss and noise factor are small (abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the first electrode of the device of Peatman on the primary surface of the second semiconductor layer as taught by Kanazawa '179 to generate a two-dimensional electron gas in a device whose conversion loss and noise factor are small.

With respect to claims 8-10, as best understood by Examiner, Peatman teaches the device as described in claim 2 above with the exception of the additional limitations:

wherein, when viewed from a perpendicular direction relative to the primary surface, the second electrode surrounds the first electrode, and the inner surface of the second electrode is formed so as to face the outer surface of the first electrode;

wherein, when viewed from a perpendicular direction relative to the primary surface, the second electrode is formed so as to surround the first electrode; and

wherein the first electrode is also formed on the primary surface of the second semiconductor layer that surrounds the first concave portion.

However, Kanazawa ‘179 teaches (FIG. 1) ohmic second electrodes (13) surrounding a Schottky first electrode (12) wherein the first electrode is formed on the primary surface of the second semiconductor layer in a device whose conversion loss and noise factor are small (abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the second electrodes of Peatman to surround the first electrode on the primary surface of the second semiconductor layer as taught by Kanazawa ‘179 in a device whose conversion loss and noise factor are small.

With respect to claim 11, as best understood by Examiner, Peatman teaches wherein a forward current passes from the first electrode to the second electrode when a voltage is applied from the first electrode to the second electrode, and a reverse current passing from the second electrode to the first electrode is restricted when the voltage is applied from the first electrode to the second electrode (p. 12, col. 1, ln. 32-48).

7. **Claims 4 and 6** rejected under 35 U.S.C. 103(a) as being unpatentable over Peatman as applied to claims 1 and 3 above, and further in view of Patel et al. (UK Patent Application Publication 2 279 806, hereinafter Patel '806) of record.

With respect to claims 4 and 6, as best understood by Examiner, Peatman teaches the device as described in claims 1 and 3 above with the exception of the additional limitations:

wherein there is further provided a second concave portion that is formed from the primary surface of the second semiconductor layer penetrating at least the second semiconductor layer and is formed from the interface to a predetermined depth in the first semiconductor layer, and wherein

the second electrode is formed on a bottom surface and side surface of the second concave portion, and forms a low resistance contact with the semiconductor layers which contact the bottom surface and side surface of the second concave portion; and

wherein the second electrode is formed from the primary surface of the second semiconductor layer to the two-dimensional carrier.

However, Patel '806 teaches forming ohmic contact layers (33) in concave portions extending beyond the interface of two semiconductor layers to the 2-DEG (15) (p. 7, ln. 21—p. 8, ln. 24) in a method to form shallow ohmic contacts extending directly to the active layer of interest in a heterojunction semiconductor device (p. 5, ln. 12-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the second electrode of Peatman in a

concave portion to the two-dimensional carrier as taught by Patel '806 to form shallow ohmic contacts extending directly to the active layer of interest in a heterojunction semiconductor device.

8. **Claims 4 and 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Peatman and Kanazawa '179 as applied to claim 2 above, and further in view of Patel '806.

With respect to claims 4 and 6, as best understood by Examiner, Peatman and Kanazawa '179 teach the device as described in claim 2 above with the exception of the additional limitations:

wherein there is further provided a second concave portion that is formed from the primary surface of the second semiconductor layer penetrating at least the second semiconductor layer and is formed from the interface to a predetermined depth in the first semiconductor layer, and wherein

the second electrode is formed on a bottom surface and side surface of the second concave portion, and forms a low resistance contact with the semiconductor layers which contact the bottom surface and side surface of the second concave portion; and

wherein the second electrode is formed from the primary surface of the second semiconductor layer to the two-dimensional carrier.

However, Patel '806 teaches forming ohmic contact layers (33) in concave portions extending beyond the interface of two semiconductor layers to the 2-DEG (15)

(p. 7, ln. 21—p. 8, ln. 24) in a method to form shallow ohmic contacts extending directly to the active layer of interest in a heterojunction semiconductor device (p. 5, ln. 12-16).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the second electrode of Peatman and Kanazawa ‘179 in a concave portion to the two-dimensional carrier as taught by Patel '806 to form shallow ohmic contacts extending directly to the active layer of interest in a heterojunction semiconductor device.

9. **Claims 8-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Peatman as applied to claims 1 and 3 above, and further in view of Kanazawa ‘179.

With respect to claims 8-10, as best understood by Examiner, Peatman teaches the device as described in claims 1 and 3 above with the exception of the additional limitations:

wherein, when viewed from a perpendicular direction relative to the primary surface, the second electrode surrounds the first electrode, and the inner surface of the second electrode is formed so as to face the outer surface of the first electrode;

wherein, when viewed from a perpendicular direction relative to the primary surface, the second electrode is formed so as to surround the first electrode; and

wherein the first electrode is also formed on the primary surface of the second semiconductor layer that surrounds the first concave portion.

However, Kanazawa '179 teaches ohmic electrodes (13) surrounding a Schottky electrode (12), wherein the Schottky electrode is formed on the primary surface of the

second semiconductor layer (11) in a device whose conversion loss and noise factor are small (abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the second electrode of Peatman to surround the first electrode as taught by Kanazawa '179; and to have formed the first electrode in the concave portion of Peatman on the primary surface of the second semiconductor as taught by Kanazawa '179 in a device whose conversion loss and noise factor are small.

10. **Claim 12** is rejected under 35 U.S.C. 103(a) as being unpatentable over Peatman as applied to claims 1 and 3 above, and further in view of Patel et al. (US Patent 5,742,077, hereinafter Patel '077).

With respect to claim 12, as best understood by Examiner, Peatman teaches the device as described in claims 1 and 3 above with the exception of the additional limitation wherein an inclination angle of the side surface of the first concave portion is equal to or greater than 10 degrees, and smaller than 90 degrees.

However, Patel '077 teaches (FIG. 1) a semiconductor device comprising deep contacts (9 and 11) formed in a concave portion having inclination angles greater than 10 degrees and smaller than 90 degrees to contact the 2DEG layer (3 and 5) (col. 2, ln. 37-59) in a device whose voltage characteristics can be altered by changing the sample geometry (col. 1, ln. 54-55).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the first concave portion of Peatman having an inclination angle equal to or greater than 10 degrees and smaller than 90 degrees as taught by Patel '077 to contact the 2D electron gas in a device whose voltage characteristics can be altered by changing the sample geometry.

11. **Claim 12** is rejected under 35 U.S.C. 103(a) as being unpatentable over Peatman and Kanazawa '179 as applied to claim 2 above, and further in view of Patel '077.

With respect to claim 12, as best understood by Examiner, Peatman and Kanazawa '179 teach the device as described in claim 2 above with the exception of the additional limitation wherein an inclination angle of the side surface of the first concave portion is equal to or greater than 10 degrees, and smaller than 90 degrees.

However, Patel '077 teaches (FIG. 1) a semiconductor device comprising deep contacts (9 and 11) formed in a concave portion having inclination angles greater than 10 degrees and smaller than 90 degrees to contact the 2DEG layer (3 and 5) (col. 2, ln. 37-59) in a device whose voltage characteristics can be altered by changing the sample geometry (col. 1, ln. 54-55).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed the first concave portion of Peatman and Kanazawa '179 having an inclination angle equal to or greater than 10 degrees and

smaller than 90 degrees as taught by Patel '077 to contact the 2D electron gas in a device whose voltage characteristics can be altered by changing the sample geometry.

Response to Arguments

12. Applicant's amendments to the claims are sufficient to overcome the prior objections to claims 3, 4, and 11 made in the final rejection filed 26 November 2008. The prior objections to claims 3, 4, and 11 have been withdrawn.

13. Applicant's amendments to the claims are sufficient to overcome the prior 35 U.S.C. 112 2nd paragraph rejections of claims 1-4, 6, and 8-11. The prior 35 U.S.C. 112 2nd paragraph rejections of claims 1-4, 6, and 8-11 have been withdrawn.

14. Applicant's arguments filed 26 February 2009 have been fully considered but they are not persuasive.

Applicant argues (remarks, p. 9) that Peatman does not at all teach (or suggest) that the third semiconductor layer is formed having a thickness that allows a quantum mechanical tunnel effect to be obtained as claimed. Examiner respectfully disagrees.

The presence of the 2-DEG layer in the device of Peatman is evidence that the AlGaAs third semiconductor layer is formed having a thickness that allows a quantum mechanical tunnel effect to be obtained. Further, Peatman discloses, "The supply [the AlGaAs third semiconductor layer] and cap [the GaAs second semiconductor layer] layers are fully depleted to the 2-DEG," (p. 12, col. 1, ln. 37-38) to demonstrate that the AlGaAs third semiconductor layer has a thickness that allows the claimed quantum

mechanical tunnel effect to be obtained. This permits the formation of an operational 2-DEG layer formed in the InGaAs first semiconductor layer.

Applicant argues (remarks, pp. 9-11) that the prior art of record does not at all teach (or suggest) that a side surface of the first concave portion is inclined against the interface as claimed. Examiner respectfully disagrees.

Peatman teaches (FIG. 1) wherein the side surface of the first concave portion is inclined against the interface (p. 12, col. 1, ln. 32-48). Peatman recites, “To form the Schottky contact, a trench is etched through to the 2-DEG layer.” In being formed in a trench and in contact with the semiconductor layers, said trench is inclined against said semiconductor layers including the interface. Though no specific angle of inclination is disclosed, FIG. 1 of Peatman shows the trench-disposed contacts having an inclination angle of approximately 90 degrees. A 90 degree inclination, or an approximation thereof, is still an inclination and is sufficient to satisfy the limitation as claimed.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Jovanovic et al. (US Patent 5,504,347) teaches forming a diode having a 2DEG from a FET having a 2DEG by omitting the gate electrode.

Beach (US Patent Application Publication 2005/0194612);

Seabaugh (US Patent 5,408,106);

Beach (US Patent Application Publication 2006/0060871);

Beach (US Patent Application Publication 2006/0065908); and

Yoshida (US Patent Application Publication 2003/0098462) teach semiconductor devices having 2DEG layers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher M. Roland whose telephone number is 571-270-1271. The examiner can normally be reached on Monday-Friday, 8:00AM-5:00PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. M. R./
Examiner, Art Unit 2893

/Davienne Monbleau/
Supervisory Patent Examiner, Art Unit 2893